In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method for ~~performing an on-board test of~~ testing connections between ~~two~~ a first programmable array circuits~~s~~ and a second programmable array circuit, comprising the steps of:

disposing a first connection circuit on ~~a~~ the first programmable array circuit according to a preset linear feedback shift register (LFSR) polynomial;

disposing a second connection circuit on ~~a~~ the second programmable array circuit according to the preset LFSR polynomial, wherein the second connection circuit has a shift register and wherein pins of the second connection circuit are connected to the corresponding pins of the first connection circuit;

inputting a test pattern to the shift register, wherein the test pattern is processed by the shift register circuit and wherein a particular pattern is produced from ~~an output pin of~~ the shift register; and

examining the particular pattern to acquire a connection status of the first and the second connection circuits.

2. (Currently amended) The method as claimed in claim 1, wherein the shift register comprises a plurality of D-type flip-flops connected in series ~~serial~~.

3. (Original) The method as claimed in claim 1, wherein a plurality of XOR gates are disposed in the first connection circuit when an LFSR circuit with the XOR gates outside the shift register is used to achieve the preset LFSR polynomial.

4. (Original) The method as claimed in claim 1, wherein a plurality of XOR gates are disposed in the second connection circuit when an LFSR circuit with the XOR gates inside the shift register is used to achieve the preset LFSR polynomial.

5. (Original) The method as claimed in claim 1, wherein the test pattern and the particular pattern are related in the form of a polynomial.

6. (Original) The method as claimed in claim 1, wherein the status includes bus speed and an appearance of cross talk.

7. (Original) The method as claimed in claim 1, wherein the programmable arrays circuits are FPGAs.

8. (Currently amended) A circuit for performing ~~an on-board test of~~ testing connections between ~~two~~ a first programmable arrays circuit~~s~~ and a second programmable arrays circuit, comprising:

a first connection circuit connected with ~~a~~ the first programmable arrays circuit; and

a second connection circuit having a shift register and connected between the first connection circuit and ~~a~~ the second programmable arrays circuit,

wherein the first and the second connection circuits are disposed according to a preset linear feedback shift register (LFSR) polynomial, wherein a test pattern is input to and processed by the shift register, and then a particular pattern is produced from ~~an output pin of~~ the shift register, and wherein the particular pattern is examined to acquire a connection status of the first and the second connection circuits.

9. (Currently amended) The method as claimed in claim 8, wherein the shift register comprises a plurality of D-type flip-flops connected in series ~~serial~~.

10. (Original) The method as claimed in claim 8, wherein the first connection circuit has a plurality of XOR gates when an LFSR circuit with the XOR gates outside the shift register is used to achieve the preset LFSR polynomial.

11. (Original) The method as claimed in claim 8, wherein the second connection circuit has a plurality of XOR gates when an LFSR circuit with the XOR gates inside the shift register is used to achieve the preset LFSR polynomial.

12. (Original) The method as claimed in claim 8, wherein the test pattern and the particular pattern are related in the form of a polynomial.

13. (Original) The method as claimed in claim 8, wherein the programmable arrays circuits are FPGAs.